CLAIMS

1. A semiconductor active backplane including an array of addressable active elements on a semiconductor substrate for selectively energising respective first electrodes of the array, wherein at least part of the region beneath a said first electrode is formed as a depletion region whereby in use it acts as a reverse biassed capacitative diode characterised in that at least one charge trapping implant is provided adjacent but spaced from said depletion region.

2. A semiconductor active backplane including an array of addressable active elements on a semiconductor substrate for selectively energising respective first electrodes of the array, wherein at least part of the region beneath a said first electrode is formed as a depletion region whereby in use it acts as a reverse biassed capacitative diode characterised in that a guard ring is provided over or around the periphery of said depletion region to prevent or hinder charge carriers from crossing between the depletion region and the rest of the substrate.

3. A semiconductor active backplane including an array of addressable active elements on a semiconductor substrate for selectively energising respective first electrodes of the array, characterised in that at least part of the region beneath a said first electrode is provided by individual capacitor plates formed beneath the electrode, one coupled to the substrate and the other coupled to the electrode.

4. A semiconductor active backplane according to any preceding claim wherein there is a single active element at each location of the array provided by a single transistor.

5. A semiconductor active backplane according to any preceding claim wherein the active element(s) have a MOS construction.

6. A semiconductor active backplane according to any preceding claim wherein substantially the whole of each active element is covered by a metallic conductor, or a pair of metallic conductors.

7. A semiconductor active backplane including an array of addressable active elements on a semiconductor substrate for energising respective first electrodes, and

first and second orthogonal sets of addressing conductors, a respective pair of addressing conductors, one from each set, being associated with the addressing of a corresponding active element, characterised in that substantially the whole of each active element is covered by a said addressing conductor in the form of a metallic conductor.

8. A semiconductor active backplane including an array of addressable active elements on a semiconductor substrate for energising respective first electrodes, and first and second orthogonal sets of addressing conductors, a respective pair of addressing conductors, one from each set, being associated with the addressing of a corresponding active element, characterised in that substantially the whole of each element is covered by a said pair of addressing conductors in the form of metallic conductors.

9. A backplane according to any preceding claim wherein the array of active elements is covered by an insulating layer, each said active element being connected to a metal electrode on said insulating layer, the array of said metal electrodes thus formed covering more than 65% of the area of said array.

10. A backplane according to any claim 9 wherein the said array of said metal electrodes covers more than 80% of the area of said array of addressable active elements.